IN THE CLAIMS

1. – 5. (Canceled)

6. (Currently Amended) The method for manufacturing a power semiconductor device according to claim ~~1~~ 10, wherein the device ~~and comprising~~ comprises at least one drain electrode contacting a face of said semiconductor substrate opposite said source regions.

7. (Currently Amended) The method for manufacturing a power semiconductor device according to claim ~~1~~ 6, wherein the device comprises ~~further comprising~~ physically isolated drain regions in the substrate and wherein said physically isolated drain regions have a depth equivalent to the depth of said base regions.

8. – 9. (Canceled)

10. (Currently Amended) A method for manufacturing a power semiconductor device comprising ~~the steps of:~~

forming a two-dimensional array of individual cells ~~on~~ from a first surface of a semiconductor substrate, each individual cell having source regions within a single and substantially uniformly doped base region surrounding said source regions of the individual cells of said array ~~base regions in the semiconductor substrate~~, and ~~characterised in that~~ forming a patterned insulated gate region at said first surface, wherein the source regions of the individual cells of the array comprise a plurality of source region branches each extending towards at least one source region branch of an adjacent cell, the source region branches of adjacent cells presenting juxtaposed ends, wherein forming said single and substantially uniformly doped base region ~~the base regions of the individual cells of the array comprising~~ comprises the steps of:

using said patterned insulated gate region in forming a ~~corresponding~~ plurality of base region branches extending radially towards at least one base region branch of an adjacent cell to present juxtaposed base region ends, ~~and~~

subsequently merging together the base region branches of adjacent cells ~~merging together~~ adjacent and between said juxtaposed base region ends to form ~~a~~ said single and substantially uniformly doped base region ~~surrounding said source regions of the individual cells of said array~~.

11. (Currently Amended) ~~A~~ The method for manufacturing a power semiconductor device as claimed in claim 0 comprising the steps of:

~~forming said base regions extending from a first surface of said semiconductor substrate with radially extending base region branches;~~

using said patterned insulated gate region in forming said source region within each base region of each individual cell with said radially extending source region branches corresponding to said base region branches.[[;]]

~~forming a gate oxide region over said first surface;~~

~~forming a source electrode in contact with said source regions of each individual cell within each of the plurality of the base regions; and~~

~~forming a drain electrode in contact with a second surface of said semiconductor substrate opposite to said first surface.~~

12. – 13. (Canceled)

14. (Currently Amended) The method of manufacturing a power semiconductor device according to claim 10 wherein forming said base regions comprises ~~the~~ a step of using said patterned insulated gate region in making ion implant of high voltage breakdown resistance for the base ~~regions~~ region branches before merging together the base region branches ~~forming a source electrode over said first surface~~.

15. (New) The method of manufacturing a power semiconductor device according to claim 10, wherein forming said base region comprises the step of causing the base region branches of adjacent cells to diffuse laterally of the array so as to merge together adjacent and between said juxtaposed ends.

16. (New) The method of manufacturing a power semiconductor device according to claim 10, wherein said source regions are formed after merging said base region branches.